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INSTITUTO ARGENTINO DE RADIOASTRONOMÍA

Digital Back-End (DBE) development at SAO for the ngEHT

G.Gancio in rep of the ngEHT DBE Design Team

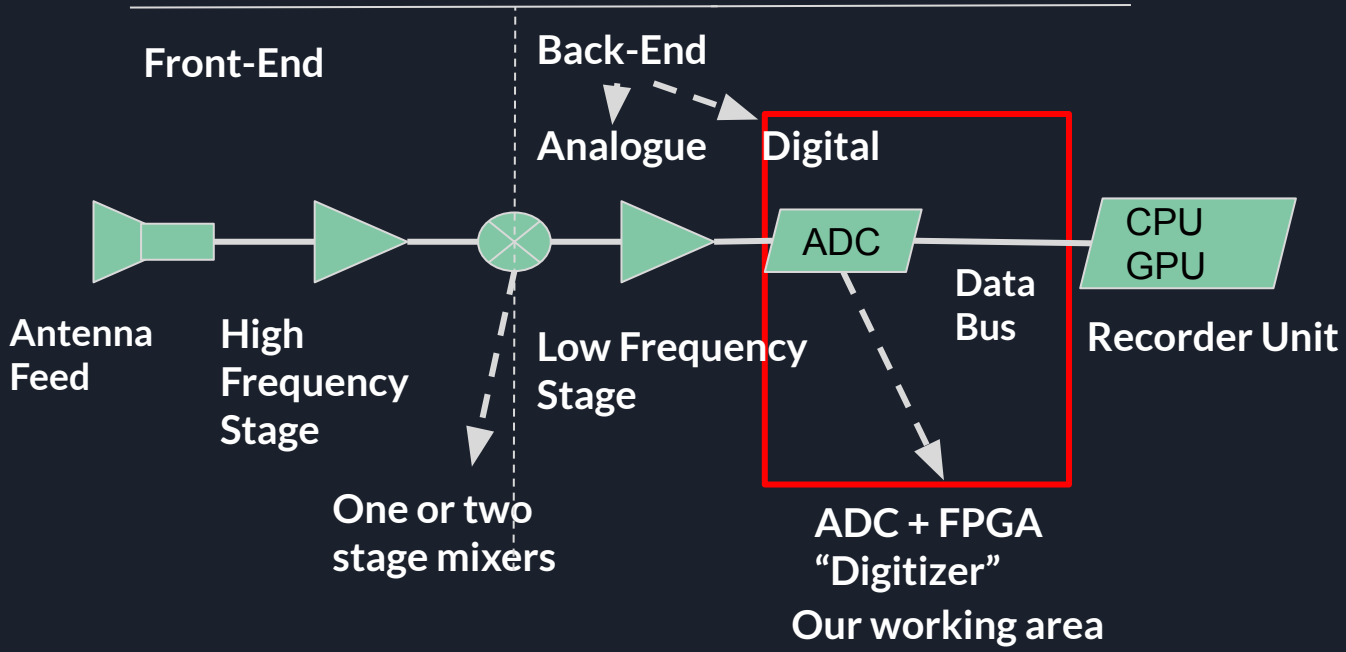
CENTER FOR ASTROPHYSICS
HARVARD & SMITHSONIAN

COGNITION
Business Intelligence

Contents

- Digital BackEnd definition
- IAR roadmap on digital backends (DBE)
- EHT vs ngEHT DBE requirements
- System block diagram of DBE
- DBE Firmware Block
- 16 Gsps ADC Characterization
- Integrated ADC/FPGA board
- Current status
  - ADC alignment (waveforms)
  - Resources used
- What's next ??
  - CMAC Interface
  - 1 Gb interface
  - Storage on a 2nd VCU128
  - Channelization

Digital Backend (DBE) Definition and main aspects



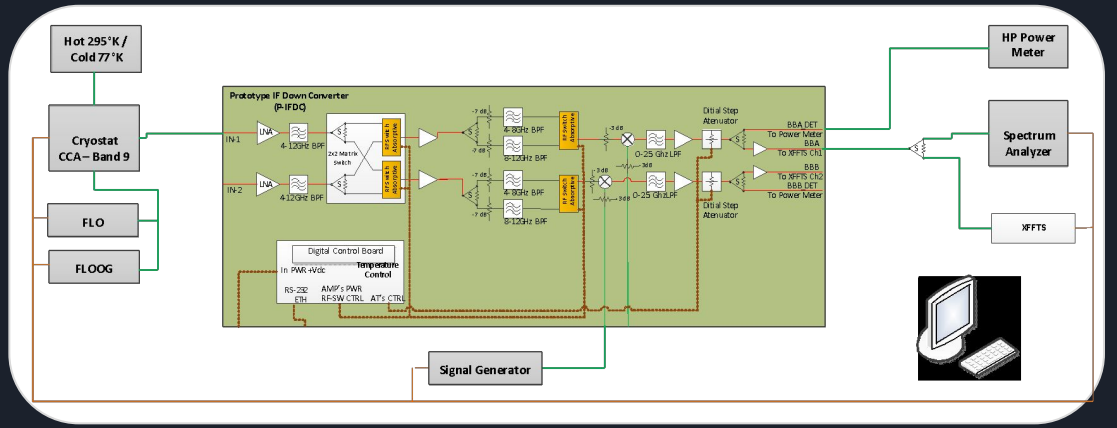
Main aspects for this talk:

- Acquisition Bandwidth
- Processing capability
- Output data rate

IAR DBEs Roadmap Highlights

2017 RPG XFFTS LLAMA Spectrometer
- 16G Hz BW Total
- Divided in 8ch 2.5GHz BW
- 8+1 1Gbps Ethernet connection

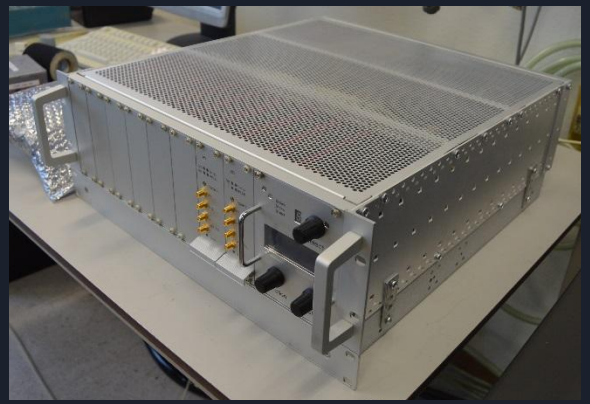
Tested at NOVA Netherlands
with Band-5 & Band-9 Submm Rxs

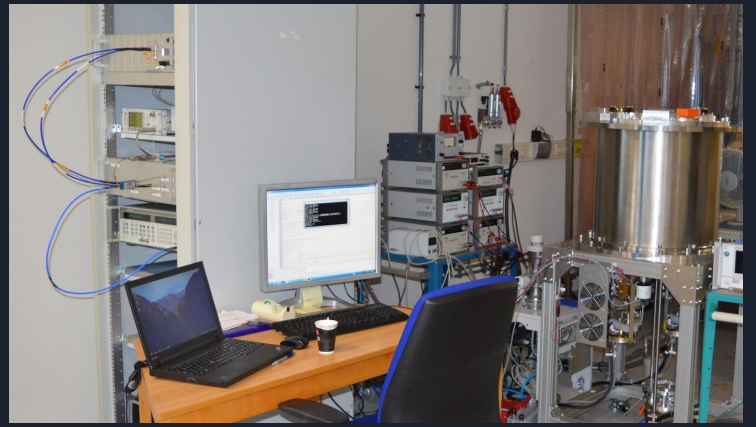


Prototype Downconverter Block Design:
J.J.Larrarte & G.Gancio - IAR
J.P. Garcia - LLAMA

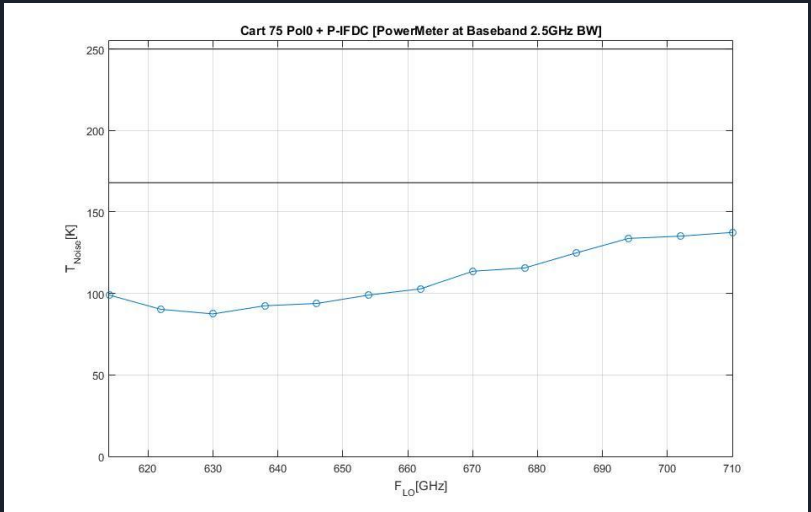
Engineer Software:
D. Zanella, - USP
F. Hauscarriaga & G. Gancio - IAR

System Integration and Test at Nova:
NOVA Team
G.Gancio - IAR
M.Luqueze - USP
S.Verri - USP

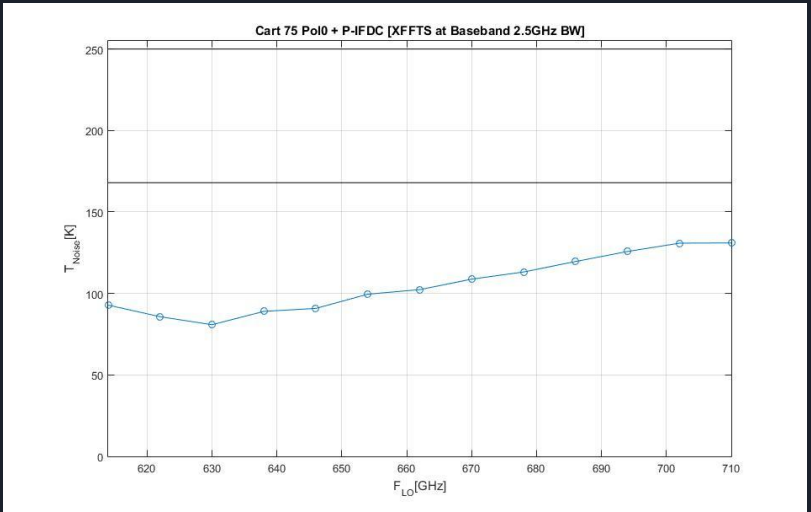




IAR DBEs Roadmap Highlights



Power Meter Readout



XFFTS Readout

IAR DBEs Roadmap Highlights

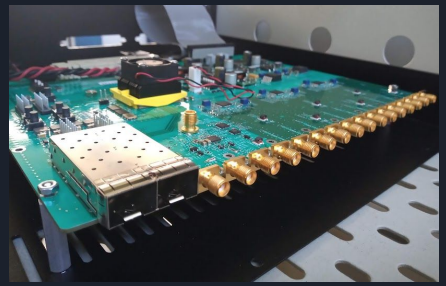
- 2018 Ettus Boards one B210, four B205 as digitizers. will all the process on CPUs. PuMa BackEnd Pulsar research.
  - 56 MHz BW Each, Data over USB 3.0 5 Gb/s [224 MHz Total BW]

- 2020 ROACH with CASPER Toolflow (IRyA - Mexico). Single Dish Pulsars, Continuum
  - x4 100 MHz BW, Data over x4 10 Gb/s [400 MHz Total BW]

- 2022 x1 SNAP Board with CASPER Toolflow, for the Multipurpose Interferometer ARRAY
  - Total of 6 Ch 250 MHz Bw To distribute, Data over x2 10 Gb/s [1.5 GHz Total BW]

- 2022 x2 RFSoC with CASPER Toolflow, for Spectral Line, Continuum experiments
  - 2 ch with 2 GHz Bandwidth each, Data over x 1Gb/s [4 GHz BW Total BW]






ngEHT DBE 2022 Team

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COGNITION Business Intelligence

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EHT vs ngEHT DBE

R2DBE EHT DBE:

- Use of ROACH-2 boards with CASPER Toolflow
- RF in 2x 2048 MHz BW [4096 MHz Total BW]
- Sampling Rate 4096 MSPS
- Total Data Rate 16 Gbps
- Xilinx FPGA Virtex-6
- Output format VDIF

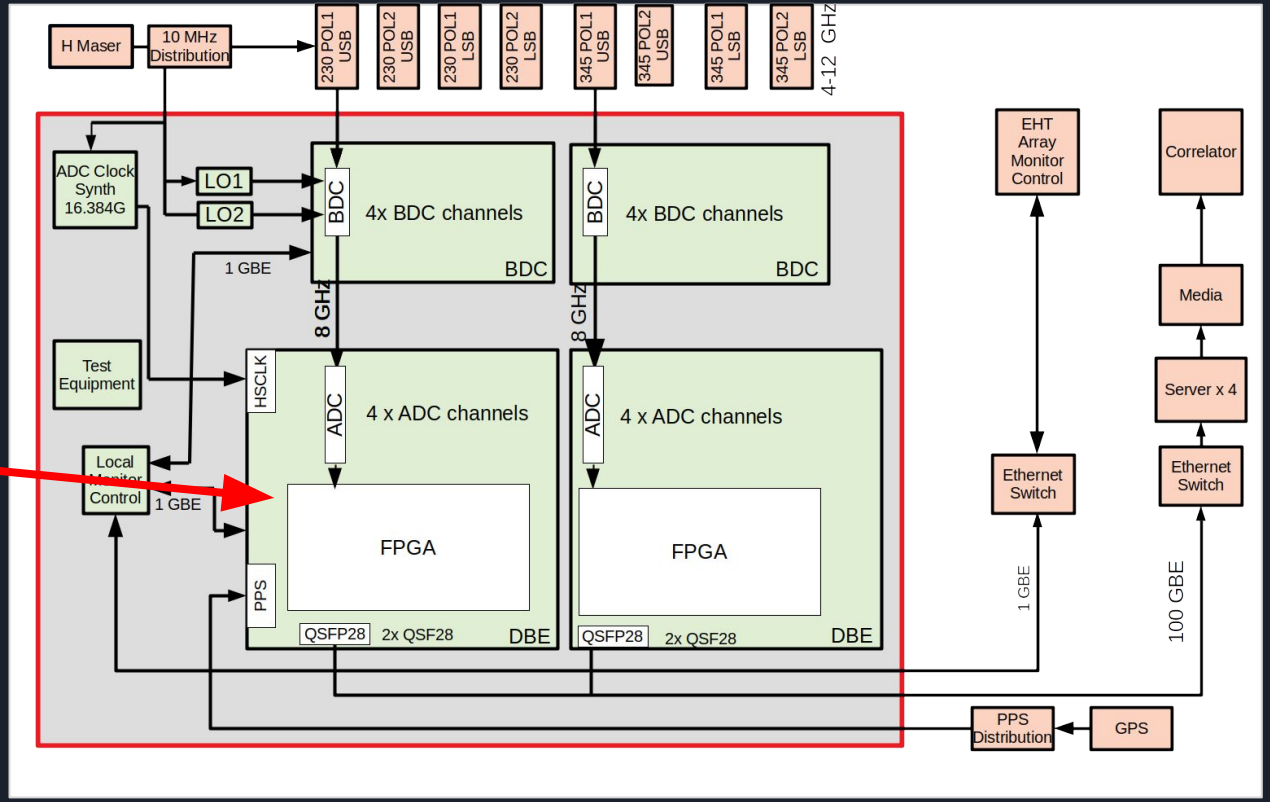
ngEHT DBE:

- Custom Board
- RF in 2x8 GHz BW [32 GHz Total BW]
- Sampling Rate 16.384 GSPS
- Total Data Rate 64 Gbps
- Xilinx FPGA Ultrascale Family
- Output format VDIF

R2DBE: A Wideband Digital Backend for the Event Horizon Telescope
http://dx.doi.org/10.1086/684513

ngEHT BackEnd Block Diagram

ngEHT DBE Board



DBE Prototype ADC board + VCUs board Setups

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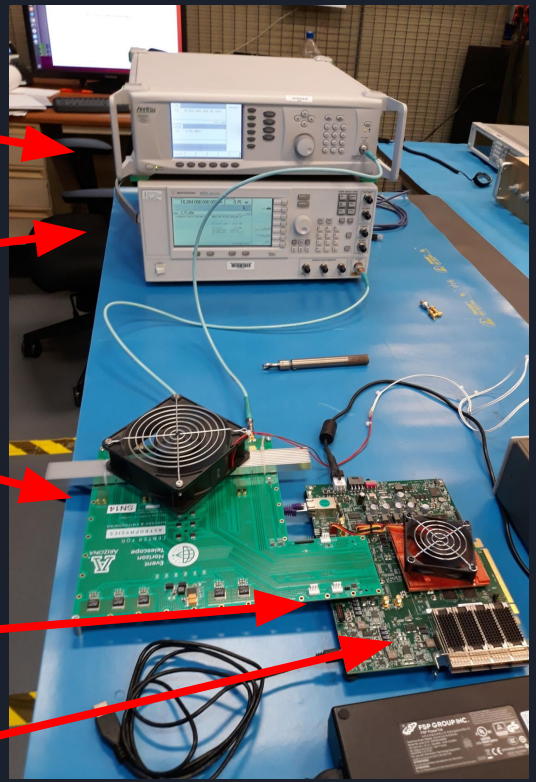
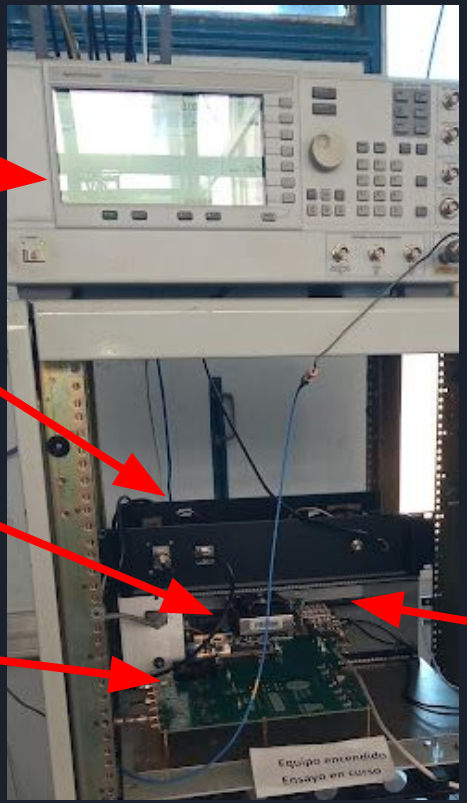
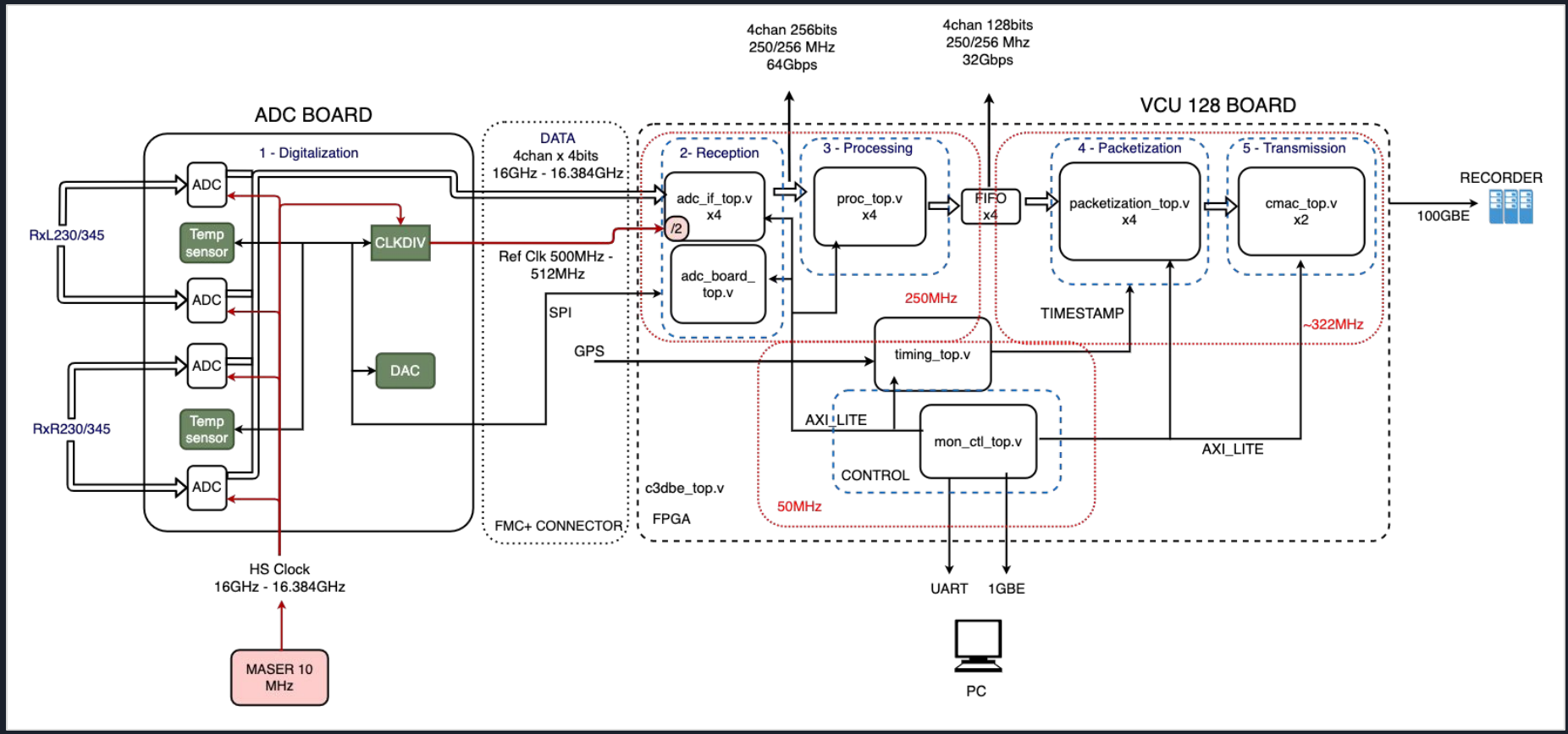


SAO Setup



IAR Setup

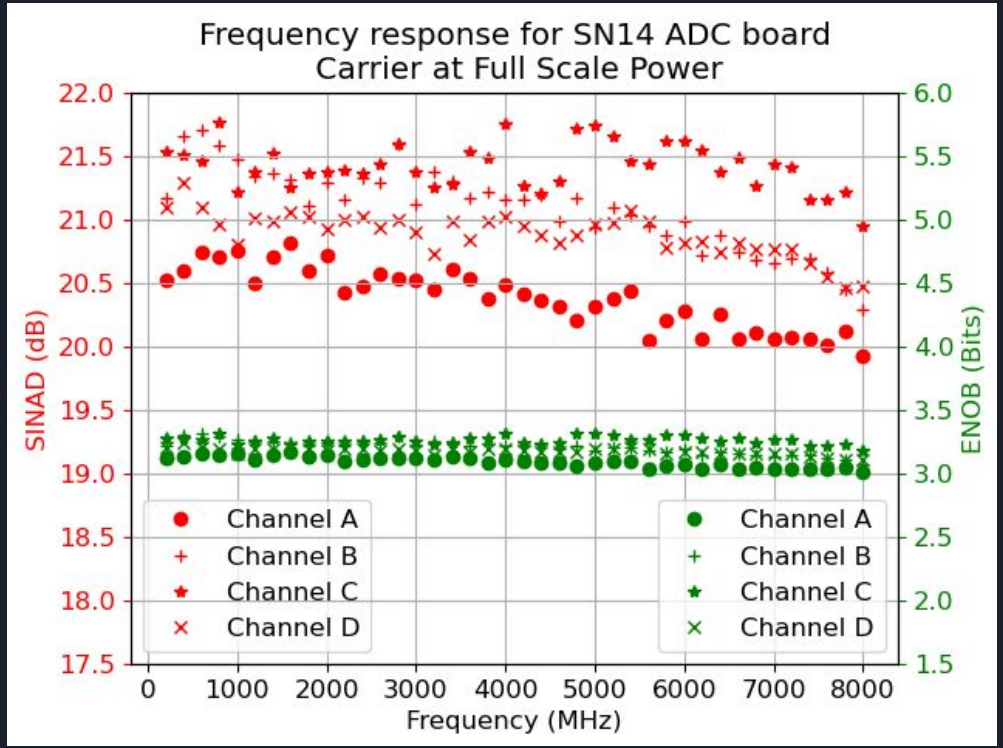
DBE Firmware



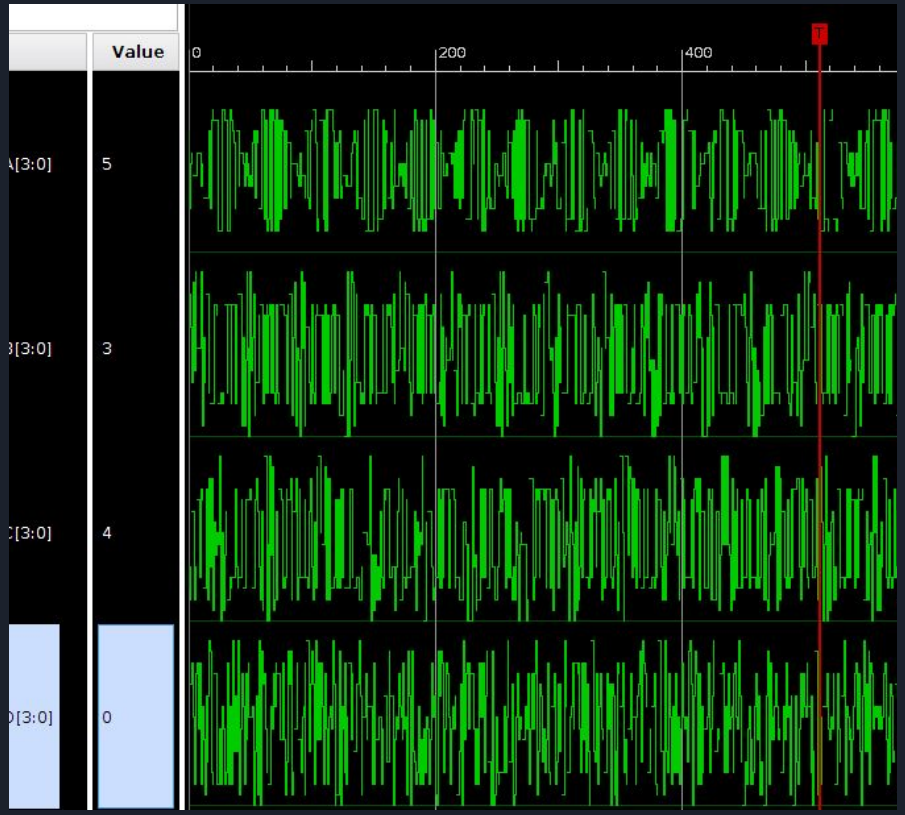
ADC Characterization

SINAD:
- Signal to Noise And Distortion

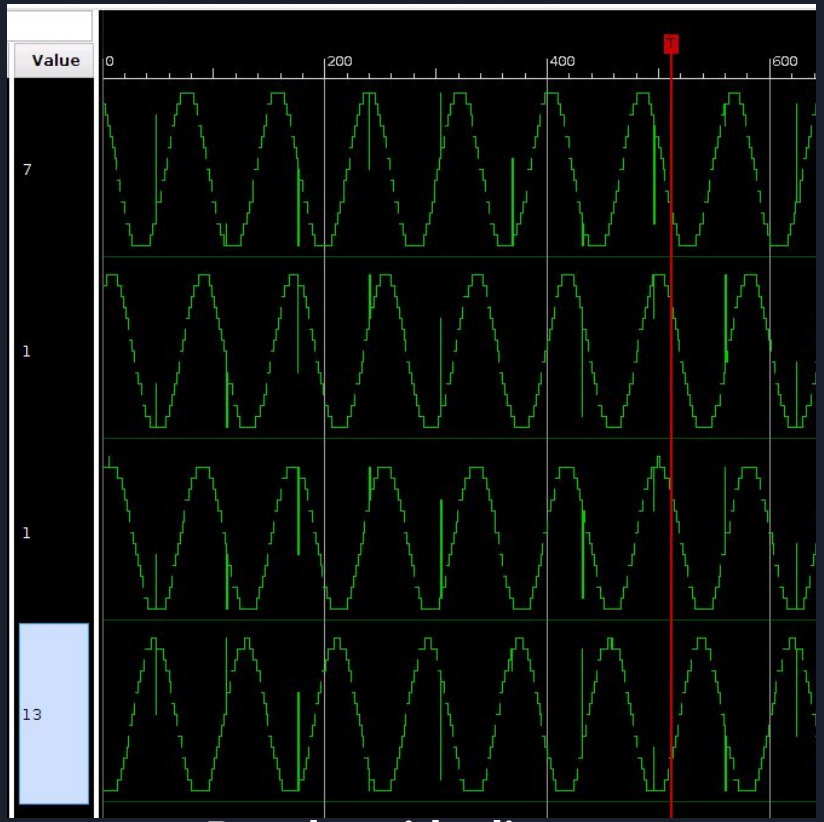
ENOB:
- Effective Number of Bits



ADC Alignment

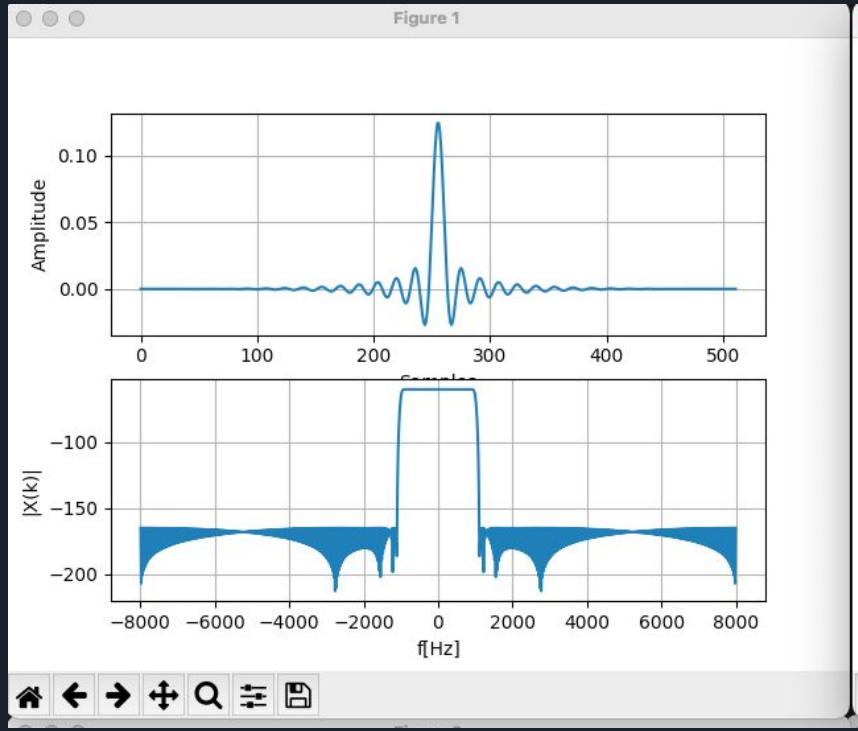


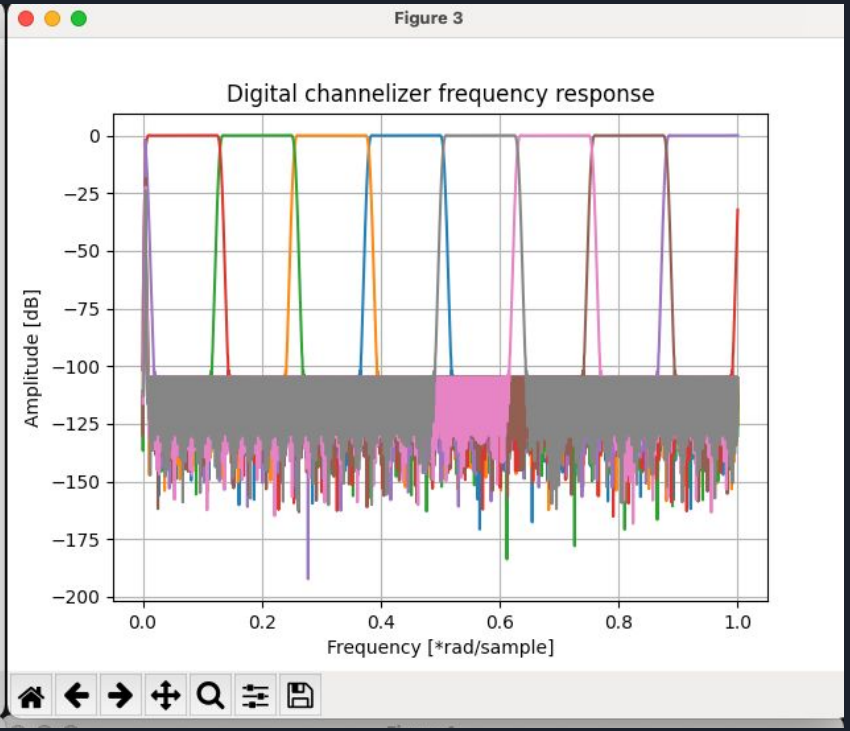
Results without alignment



Results with alignment

Channelization





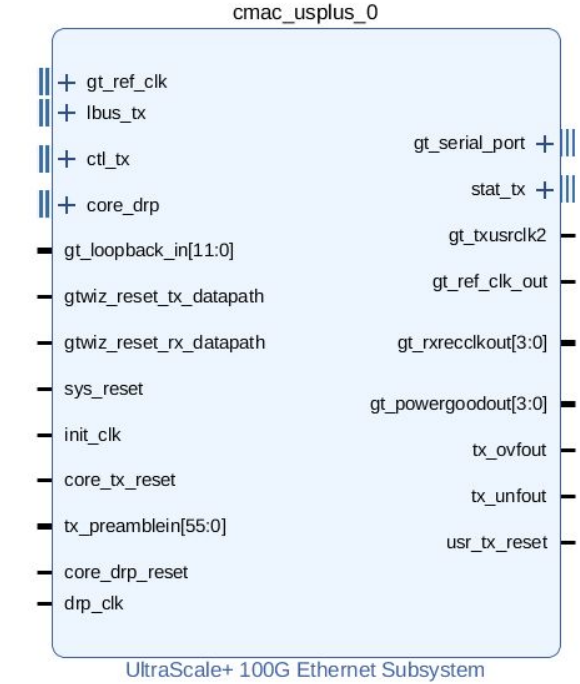
100 Gbps CMAC Interface

- **What has been done?**

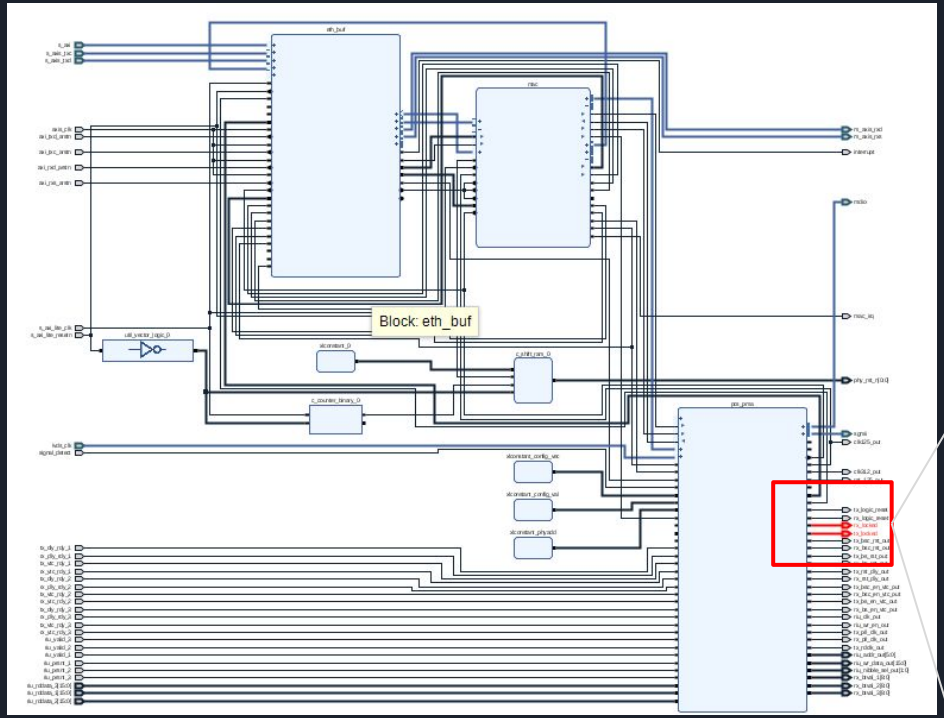
At this point there hasn't been any packet loss, which means that every packet sent to the MAC is being accepted and transferred to the PHY

- **What is still to cover?**

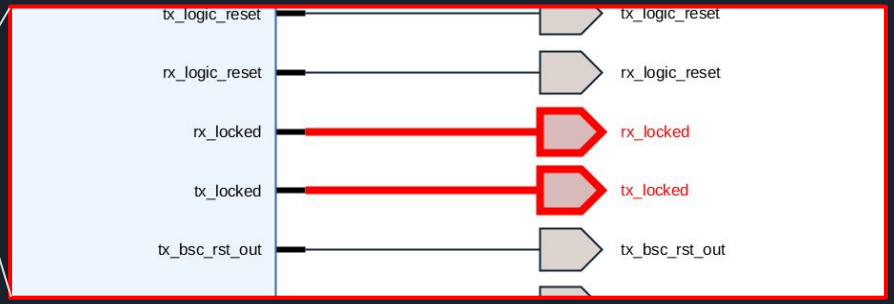
The connection between the switch and the FPGA is off because we need a licence by Xilinx to bring up the copper based mediums link



1Gb Ethernet Interface

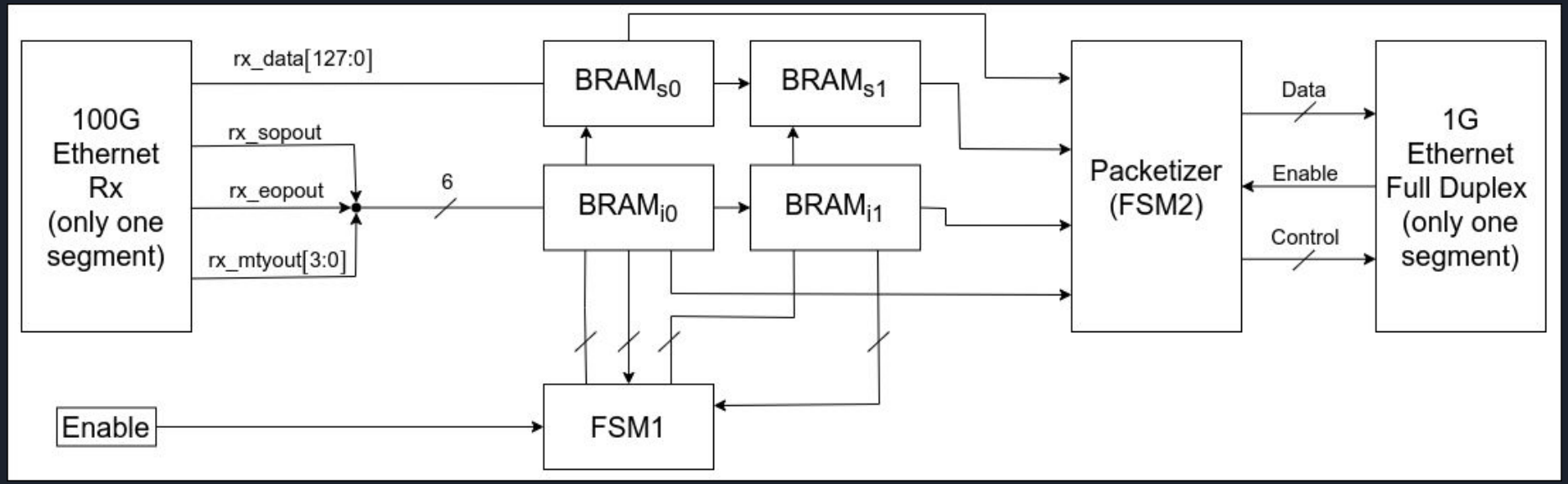


The 1 Gb Ethernet is currently being debugged because some intermittency was found in the signal provided by the following pins. We've come to the conclusion that this may be the cause of the issue related to the bad connection through this interface.



© Xilinx Inc. Vivado IDE. AXI 1G/2.5G Ethernet Subsystem

Storage (Separate VCU128)



Integrated PCB vs Available Boards

Why not use the 4 channel ADC board + VCU128 ??

- FMC+ connector not a reliable high speed connector
- Having intermittent connectivity issues with the 1 Gb
- Not sure about performance when board resources start to get used up (DSP slices)
- Several resources not being used that Consumes lots of Power (PCIe, Transceivers, Clocks)
- Difficult to comply with thermal dissipation

A new PCB will:

- Integrate in a single board the ADCs and FPGA with a better signal integrity
- Take into consideration thermal issues for a good heat dissipation
- Less power consumption by removing all unnecessary electronics (PCIe, Transceivers, etc)
- Better housekeeping design for telemetry control.

Design Team for the PCB has started the design process

Conclusions

- The DBE prototype should be delivered End 2022 / Beginning 2023
- We are expecting to measure the throughput in the near future.
- We are hoping to have a custom board for the FPGA/ADC for the fringe test.
- We are hoping to have a scaled down channelized version of the firmware also for the fringe test.
- A system integration end to end test must be performed with the Block Down Converter (BDC) and DBE before the OVRO/LMT fringe test. (End of 2023)